WHAT IS CLAIMED IS:

1. A differential amplifier circuit comprising:

(a) first and second supply voltage rails, first and second input terminals, and an output terminal;

(b) differentially connected first and second input transistors of a first channel type;

(c) a folded cascode circuit coupled to the first supply voltage rail and including a first cascode transistor and a second cascode transistor both of a second channel type, sources of the first and second cascode transistors being coupled to drains of the first and second input transistors, respectively;

(d) a first load transistor of the second channel type coupled between the source of the second cascode transistor and the first supply voltage rail and a second load transistor of the second channel type coupled between the source of the first cascode transistor and the first supply voltage rail;

(e) a bias source producing a bias signal on gates of the first and second cascode transistors;

(f) a third cascode transistor of the second channel type having a source coupled to a drain of the second cascode transistor and a drain coupled to a first current source, a drain of the first cascode transistor being coupled to a second current source, and a voltage level shift circuit coupled between the drain of the third cascode transistor and second load transistors; and

(g) a gain boost amplifier having a first input coupled to the drain of the first cascode transistor, a second input coupled to the drain of the second cascode transistor, and an output coupled to a gate of the third cascode transistor.

2. The differential amplifier circuit of claim 1 including an output stage having an input coupled to the drain of the first cascode transistor, the output stage including a pull-up transistor of the second channel type coupled between the second supply voltage rail and the output terminal, and a second output transistor of the first channel type coupled between the first supply voltage rail and the output terminal.

3. The differential amplifier of claim 2 including a class AB bias circuit coupled between a gate electrode of the pull-up and a gate electrode of the pull-down transistor.

4. The differential amplifier of claim 2 wherein the gain boost amplifier is a CMOS voltage-input differential amplifier.

5. The differential amplifier of claim 2 wherein the gain boost amplifier is a CMOS current-input differential amplifier.

6. A differential amplifier circuit comprising:

(a) first and second supply voltage rails, first and second input terminals, and

an output terminal;

(b) differentially connected first and second input transistors of a first channel type;

(c) a folded cascode circuit coupled to the first supply voltage rail and including a first cascode transistor and a second cascode transistor both of a second channel type, sources of the first and second cascode transistors being coupled to drains of the first and second input transistors, respectively;

(d) a first load transistor of the second channel type coupled between the source of the second cascode transistor and the first supply voltage rail and a second load transistor of the second channel type coupled between the source of the first cascode transistor and the first supply voltage rail;

(e) a bias source producing a bias signal on gates of the first and second cascode transistors, respectively; and

(f) a gain boost amplifier having a first input coupled to the drain of the second cascode transistor, a second input coupled to the drain of the first cascode transistor, and an output coupled to gates of the first and second load transistors.

7. The differential amplifier circuit of claim 6 including an output stage having an input coupled to the drain of the first cascode transistor, the output stage including a pull-up transistor of the second channel type coupled between the second supply voltage rail and the output terminal, and a second output transistor of the first channel type coupled between the first supply voltage rail and the output terminal.

8. The differential amplifier of claim 7 including a class AB bias circuit coupled between a gate electrode of the pull-up and a gate electrode of the pull-down transistor.

9. The differential amplifier of claim 7 wherein the gain boost amplifier is a CMOS voltage-input differential amplifier.

10. The differential amplifier of claim 7 wherein the gain boost amplifier is a CMOS current-input differential amplifier.

11. A differential amplifier circuit comprising:

(a) first and second supply voltage rails, first and second input terminals, and an output terminal;

(b) differentially connected first and second input transistors of a first channel type;

(c) a folded cascode circuit coupled to the first supply voltage rail and including a cascode transistor of a second channel type, a source of the cascode transistor being coupled to a drain of the first input transistor;

(d) a first load transistor of the second channel type coupled between a first current source and the first supply voltage rail and a second load transistor of the second channel type coupled between the source of the cascode transistor and the first supply voltage rail;

(e) a bias source producing a bias signal on a gate of the cascode transistor;

and

(f) a gain boost amplifier having a first input coupled to a drain of the first load transistor, a second input coupled to the source of the cascode transistor, and an output coupled to gates of the first and second load transistors.

12. The differential amplifier circuit of claim 11 including an output stage having an input coupled to the drain of the first cascode transistor, the output stage including a pull-up transistor of the second channel type coupled between the second supply voltage rail and the output terminal, and a second output transistor of the first channel type coupled between the first supply voltage rail and the output terminal.

13. The differential amplifier of claim 12 including a class AB bias circuit coupled between a gate electrode of the pull-up and a gate electrode of the pull-down transistor.

14. The differential amplifier of claim 12 wherein the gain boost amplifier is a CMOS voltage-input differential amplifier.

15. The differential amplifier of claim 12 wherein the gain boost amplifier is a CMOS current-input differential amplifier.

16. A differential amplifier circuit comprising:

(a) first and second supply voltage rails, first and second input terminals, and an output terminal;

(b) differentially connected first and second input transistors of a first channel type;

(c) a first load transistor of a second channel type coupled between a drain of the first input transistor and the first supply voltage rail and a second load transistor of the second channel type coupled between a drain of the second input transistor and the first supply voltage

rail; and

(d) a gain boost amplifier having a first input coupled to the drain of the first input transistor, a second input coupled to the drain of the second input transistor, and an output coupled to gates of the first and second load transistors.

17. The differential amplifier circuit of claim 16 including an output stage having an input coupled to the drain of the first cascode transistor, the output stage including a pull-up transistor of the second channel type coupled between the second supply voltage rail and the output terminal, and a second output transistor of the first channel type coupled between the first supply voltage rail and the output terminal.

18. The differential amplifier of claim 17 including a class AB bias circuit coupled between a gate electrode of the pull-up and a gate electrode of the pull-down transistor.

19. The differential amplifier of claim 17 wherein the gain boost amplifier is a CMOS voltage-input differential amplifier.

20. The differential amplifier of claim 17 wherein the gain boost amplifier is a CMOS current-input differential amplifier.

21. A method of operating a differential amplifier circuit which includes first and second supply voltage rails, first and second input terminals, and an output terminal, differentially connected first and second input transistors of a first channel type, and a folded cascode circuit coupled to the first supply voltage rail and including a first cascode transistor and a second cascode transistor both of a second channel type, sources of the first and second cascode transistors being coupled to drains of the first and second input transistors, respectively, the sources of the first and second cascode transistors also being coupled to a drain of a first load transistor and a drain of a second load transistor, respectively, the method comprising:

boosting the gain of the differential amplifier circuit without introducing additional components into a signal path of the differential amplifier circuit by providing local feedback

representative of an output voltage of the differential amplifier circuit to gates of the first and second load transistors by

(a) coupling a drain of a third cascode transistor of the second channel type to a current source circuit and coupling a source of the third cascode transistor to a drain of the second cascode transistor;

(b) coupling a drain of the third cascode transistor to gates of the first and second load transistors; and

(c) driving a gate of the third cascode transistor by means of a gain boost amplifier having a first input coupled to the drain of the first cascode transistor and a second input coupled to the drain of the second cascode transistor, to accomplish the function of increasing the output impedance of the differential amplifier circuit.

22. The method of claim 21 wherein step (b) includes driving a gate of the third cascode transistor by means of a level shift circuit coupled to the drain of the third cascode transistor.

23. A method of operating a differential amplifier circuit which includes first and second supply voltage rails, first and second input terminals, and an output terminal, differentially connected first and second input transistors of a first channel type, and a folded cascode circuit coupled to the first supply voltage rail and including a first cascode transistor and a second cascode transistor both of a second channel type, sources of the first and second cascode transistors being coupled to drains of the first and second input transistors, respectively, the sources of the first and second cascode transistors also being coupled to a drain of a first load transistor and a drain of a second load transistor, respectively, the method comprising:

boosting the gain of the differential amplifier circuit without introducing additional components into a signal path of the differential amplifier circuit by providing local feedback representative of an output voltage of the differential amplifier circuit to gates of the first and second load transistors by

(a) coupling a first input of a gain boost amplifier to a drain of the first cascode transistor, and coupling a second input of the gain boost amplifier to a drain of the second cascode transistor; and

(b) coupling an output of the gain boost amplifier to gates of the first and second load transistors to drive the first and second load transistors so as to accomplish the function of increasing the output impedance of the differential amplifier circuit.

24. A method of operating a differential amplifier circuit which includes first and second supply voltage rails, first and second input terminals, and an output terminal, differentially connected first and second input transistors of a first channel type, and a folded cascode circuit coupled to the first supply voltage rail and including a first cascode transistor and a second cascode transistor both of a second channel type, sources of the first and second cascode transistors being coupled to drains of the first and second input transistors, respectively, the sources of the first and second cascode transistors also being coupled to a drain of a first load transistor and a drain of a second load transistor, respectively, the method comprising:

boosting the gain of the differential amplifier circuit without introducing additional components into a signal path of the differential amplifier circuit by providing local feedback representative of an output voltage of the differential amplifier circuit to gates of the first and second load transistors by

(a) coupling a first input of a gain boost amplifier to the source of the first cascode transistor, and coupling a second input of the gain boost amplifier to the source of the second cascode transistor;

(b) coupling a drain of the second cascode transistor to gates of the first and second load transistors; and

(c) coupling an output of the gain boost amplifier to a gate of the second cascode transistor to cause the drain of the second cascode transistor to drive the gates of the first

and second load transistors so as to accomplish the function of increasing the output impedance of the differential amplifier circuit.

25. A method of operating a differential amplifier circuit which includes first and second supply voltage rails, first and second input terminals, and an output terminal, differentially connected first and second input transistors of a first channel type, sources of the first and second input transistors being coupled to the drain of a first load transistor and a drain of a second load transistor, respectively, the method comprising:

boosting the gain of the differential amplifier circuit by providing local feedback representative of an output voltage of the differential amplifier circuit to gates of the first and second load transistors by

(a) coupling a first input of a gain boost amplifier to a drain of the first load transistor, and coupling a second input of the gain boost amplifier to a drain of the second load transistor; and

(b) coupling an output of the gain boost amplifier to gates of the first and second load transistors to drive the first and second load transistors so as to accomplish the function of increasing the output impedance of the differential amplifier circuit.

26. A current mirror circuit comprising:

(a) a supply voltage rail, an input terminal, and an output terminal;

(b) a first transistor and a second transistor;

(c) a third transistor coupled between a source of the first transistor and the supply voltage rail and a fourth transistor coupled between a source of the second transistor and the supply voltage rail;

(d) a first bias source producing a bias signal on gates of the first and second transistors, respectively;

(e) a fifth transistor having a source coupled to a drain of the first transistor and a drain coupled to the input terminal, a drain of the second transistor being coupled to the output terminal, and a second bias source coupled to gates of the third and fourth transistors; and

(f) an amplifier having a first input coupled to the drain of the second transistor, a second input coupled to the drain of the first transistor, and an output coupled to a gate of the fifth transistor.